OpenCAPI vs OMI Comparison

TLx Comparison(s)

Transaction Layer (TLx) Version	Physical Form Factor	Protocols	Protocol Description
3.0	PCIe Add-In Card	C1, M0 C1, M1 C0, M1	Non-Caching DMA Non- Caching DMA + LPC LPC
3.1 (OMI)	DDIMM	Memory Controller	
4.0	PCIe Add-In Card	C1, M0 C1, M1 C0, M1 C2, M0 C2, M1	Non-Caching DMA Non- Caching DMA + LPC LPC Accelerator Cache Accelerator Cache + LPC

DLx Comparison(s)

DataLink Layer (DLx) Version	Physical Form Factor	Rate Gbps	Ref Clock MHz	Transmission Mode	Idle Flit Length	Error Detection Per Lane
3.0	PCIe Add-In Card	25.78125	156.25	Store and Forward	Long Idles	No
3.1 (OMI)	DDIMM	25.6/21.33	133.33	Low Latency	Short Idles	Yes
4.0	PCIe Add-In Card	31.875/25.78125	156.25	Dependent on Implementation	Dependent on Implementation	Dependent on Implementation
	DDIMM	32.0	133.33	Low Latency Mode	Short Idles	Yes

Power Processor Implementations

Processor Family	Transaction Layer (TL) Version	DataLink Layer (DL) Version	Physical Form Factor	Rate Gbps	Ref Clock MHz
Power9	3.0	3.0	PCIe Add-In Card	25.78125	156.25
Power9’ (Axone)	4.0 3.1 (OMI)	3.0 3.1 (OMI)	PCIe Add-In Card DDIMM	25.78125 25.6/21.33	156.25 133.33
Power10	4.0 3.1 (OMI)	4.0 3.1 (OMI)	PCIe Add-In Card DDIMM	25.78125 25.6/21.33	156.25 133.33

OMI Minimum Command Set

TL Command Ie Processor Initiated	Requirement
config_read	M
config_write	M
intrp_rdy	M.ir
mem_cntl	O
nop	M
pad_mem	O
pr_rd_mem	M
pr_wr_mem	M
rd_mem	M
rd_pf	M
write_mem	M
write_mem.be	M

TLx Command Ie Memory Buffer Initiated	Requirement
assign_actag	M
intrp_req	M
intrp_req.d	M
nop	M

M.ir = Mandatory if AFU issues any form of of intrp_req
Otherwise Unsupported

See Chapters 2.2 and 2.3 of the TL 3.1 Specification for details

OMI Minimum Response Set

TL Response Ie Processor Responses	Requirement
intrp_resp	M.ir
nop	M
return_tlx_credits	M

M.Ir = Mandatory if AFU issues any form of intrp_req
Otherwise Unsupported

See Chapters 2.4 and 2.5 of the TL 3.1 Specification for details

TLx Responses Ie Memory Buffer Responses	Requirement
mem_rd_fail	M
mem_rd_response	M
mem_rd_response.ow	M.a
mem_rd_response.xw	M.b
mem_wr_fail	M
mem_wr_response	M
nop	M
return_tl_credits	M

M.a = Mandatory if templates x'07' or x'09' are supported
M.b = Mandatory if template x'08' is supported

OMI Minimum Template Sets

TLx Receive (ie Memory Buffer) TL Transmit (ie Processor)	Requirement
x'00'	M
x'01	O
x'04'	O
x'07'.a	O
x'0A'.b	O

TL Receive (ie Processor) TLx Transmit (ie Memory Buffer)	Requirement
x'00'	M
x'01'	O
x'05'	O
x'09'.c	O
x'0B'.d	O

To support metadata, an implementation must support one of the following templates: x'04', x'05' or x'06'

x'07'.a = This template is used to support 32-byte data carriers

x'0A'.b = This template is used to support 32-byte data carriers with extended-metadata

See Chapters 6.1 and 6.2 of the TL 3.1 Specification for details

To support metadata, an implementation must support one of the following templates: x'04', x'05' or x'06'

x'09'.c = This template is used to support 32-byte data carriers

x'0B'.d = This template is used to support 32-byte data carriers with extended-metadata