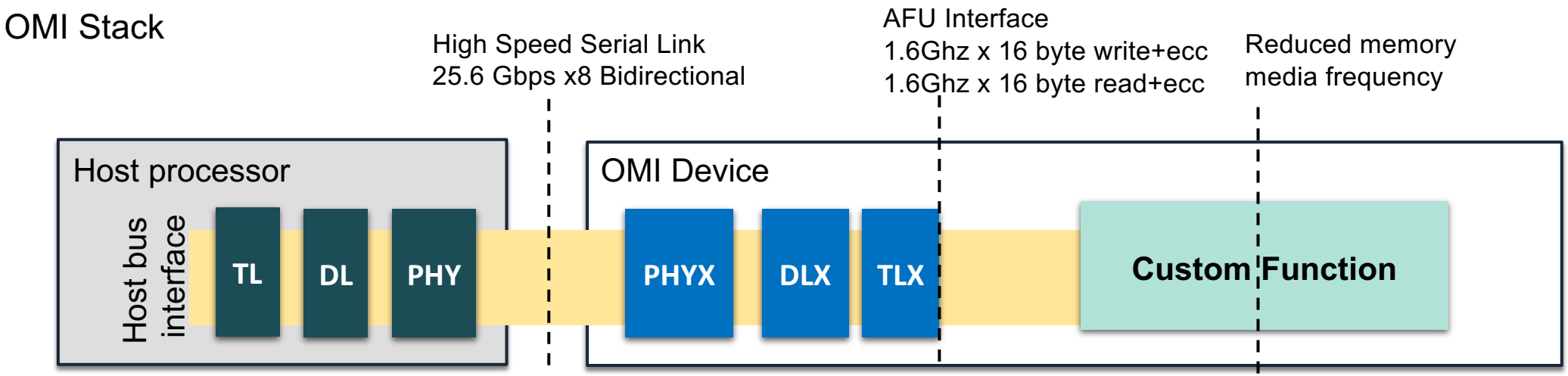
# Current Open Memory Interface (OMI) Reference




- ASIC DLX/TLX RTL
  - Open Source forthcoming
- FPGA Host emulator (3.1)
  https://github.com/OpenCAPI/omi_host_fire
- FPGA Device emulator (3.1)
  https://github.com/OpenCAPI/omi_device_ice

DLX

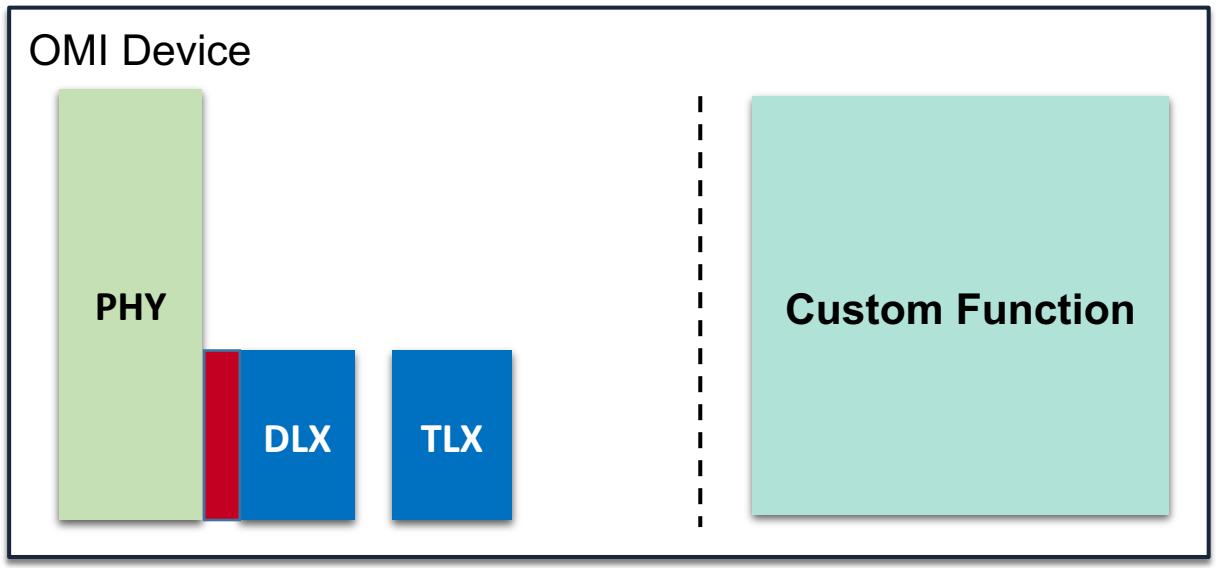
Serial to parallel
Training
Scramble
Replay
CRC Gen / Check

TLX

Frame decoder
TL parser
TL response

- OMI and PCIe PHY are compatible/interoperable
  - OMI PHY layer is Based on the OIF CEI 28G SR specification
  - PCIe 5 SerDes PHY x16
  - OMI 32 Gbps PHY x8
  - OMI reference clock is 133.33 MHz
  - PCIe reference clock is 100 MHz
- OMI 3.1 available with P10

The DLX of OMI
Is directly connected to the serdes pins of the PHY
No connection to PCS/PIPE as in the PCI-e stack



# DL <-> PHY Interface

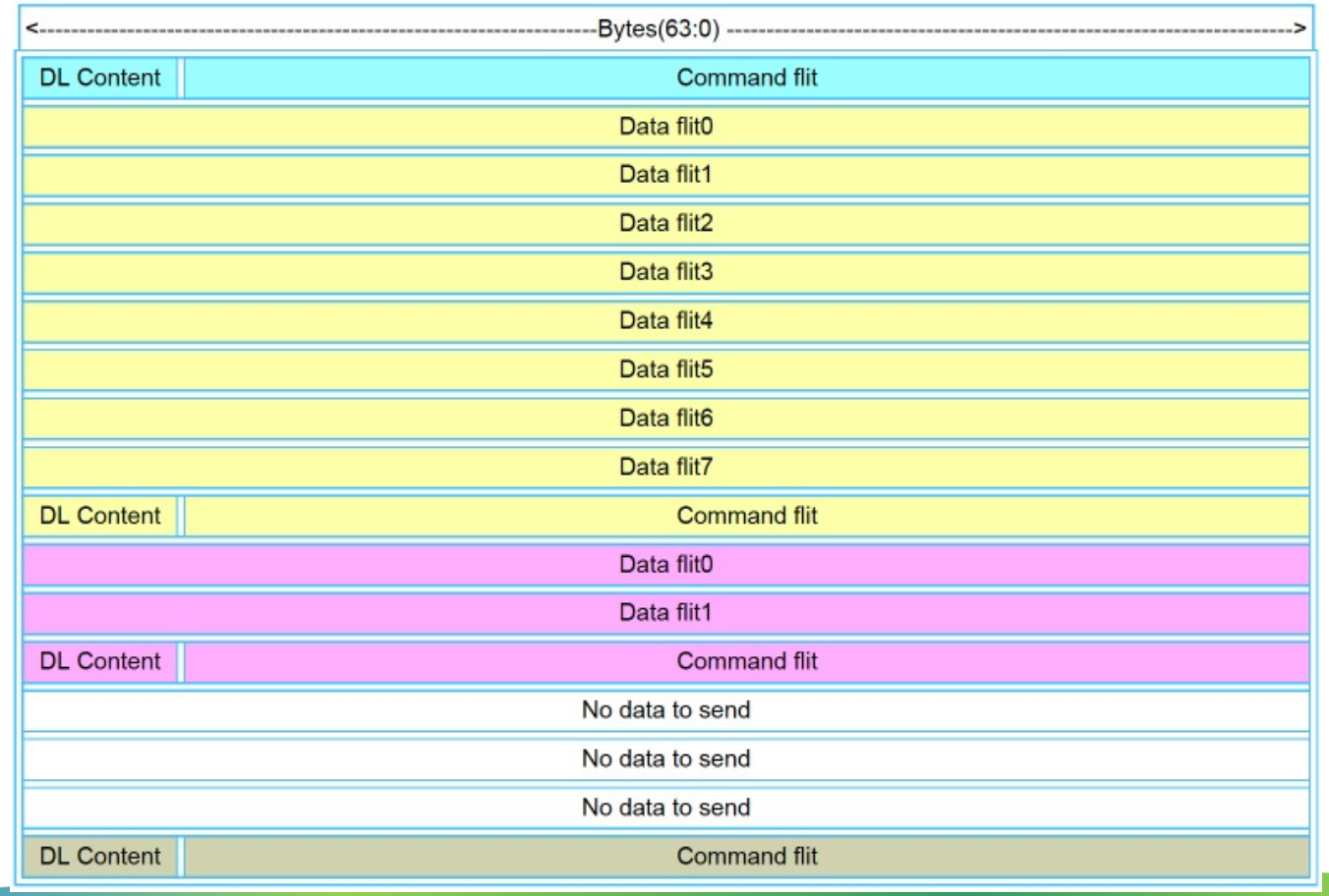
| DL <-> PHY Signal | Comment |
|---|---|
| PHY_DL_CLOCK_<7:0> | Recovered captured clock for this lane |
| PHY_DL_LANE_<7:0>(15:0) | 16 bits of Rx Data for this lane |
| PHY_DL_INIT_DONE_<7:0> | Indication from the PHY that it is trained and has good eyes |
| PHY_DL_RECAL_DONE_<7:0> | Indication from the PHY that calibration is complete |
| PHY_DL_IOBIST_RESET | Reset to the DL driven from the PHY to kick off IOBIST |
| PHY_DL_RX_PSAVE_STS_<7:0> | Indicates if the Rx Lane has responded to a Power Saving Request and is in Low Power State |
| PHY_DL_TX_PSAVE_STS_<7:0> | Indicates if the Tx Lane has responded to a Power Saving Request and is in Low Power State |
| DL_PHY_IOBIST_PRBS_ERROR(7:0) | DL to PHY to indicate a PRBS error |
| DL_PHY_LANE_<7:0>(15:0) | 16 bits of Tx Data for this lane |
| DL_PHY_RUN_LANE_<7:0> | Indication to the PHY to run in high speed mode |
| DL_PHY_TX_PSAVE_REQ_<7:0> | Indication to the PHY to turn off the driver logic to save power |
| DL_PHY_RX_PSAVE_REQ_<7:0> | Indication to the PHY to turn off the receiver logic to save power |
| DL_PHY_RECAL_REQ_<7:0> | Indication to the PHY to run calibration on this lane |

# Data Link Layer Overview

- Handles raw data packets as they arrive and depart through the physical interface
- Data alignment between lanes
- Maintains frame lock
- Handles replay when errors are detected
- 16:1 frequency ratio between PHY and DL
- Scrambles data to prevent loss of phase lock in receiving PHY
- Synchronization header
  - Specifies data units (flits) versus link control payloads

# Data Link Layer Frames

- **64 bytes in size**
- **Command flits include ‘DL Content’**
- **Up to 8 data flits for each command flit**
- **Control flits contain CRC information for the prior data flits**




| | |
|---|---|
| DL Content | Command flit |
| Data flit0 | |
| Data flit1 | |
| Data flit2 | |
| Data flit3 | |
| Data flit4 | |
| Data flit5 | |
| Data flit6 | |
| Data flit7 | |
| DL Content | Command flit |
| Data flit0 | |
| Data flit1 | |
| DL Content | Command flit |
| No data to send | |
| No data to send | |
| No data to send | |
| DL Content | Command flit |

# Data Content

- **Cyclic Redundancy Code – Protects control flit and up to prior 8 data flits**
- **ACK Count – Number of flits received since last DL Content**
  - **Helps with replay**
- **DL2DL ACK – Power management control**
- **TL Template – Which TL template type generated info in rest of control flit**
- **Bad Data – Indicates when problems occur with data flits**
- **Run Length – Number of subsequent data flits to expect**

| Bits | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 |
| 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC(35:20) | | | | | | | | | | | | | | | |
| CRC(19:4) | | | | | | | | | | | | | | | |
| CRC(3:0) | | | | ACK Count(4:0) | | | | | DL2DL ACK(1:0) | | Reserved | | | | TL Tem-plate(5:4) |
| TL Template(3:0) | | | | Bad Data Flit(7:0) | | | | | | | | | Run Length(3:0) | | |

# Transaction Layer Overview


- Receives DL frames from DL receiver
  - Buffers flits (16 bytes) to create OpenCAPI frames (64 bytes)
- Sends DL frames back to DL transmitter
- Handles higher-level command and data
- Flow control management using credits
- Various templates available for mixing data and control information together